**Design of low power cache memory using 4T SRAM for SoC designs**

**Motivation:**

Power and area reduction in embedded systems, which use SoC designs, is main aim of VLSI design. This project deals with the reduction in power and area consumed by memory in SoC with acceptable trade off of stability and performance.

SoCs integrate multiple functions on a single silicon die. As process geometries have scaled, designs which use more and more of the additional silicon real estate available on chips to integrate embedded memories evolved. These embedded memories allow for significantly better system performance and lower power compared to a solution where off-chip memories are used. Most current designs have over 50% of their area used by embedded memories and these memories account for 50-70% of the total SoC power dissipation. Clearly, any attempt to reduce SoC power is incomplete if it does not attempt to reduce the power consumed by the embedded memories in the design.

Most memories embedded in SoCs are static RAMs. In order to achieve lower power consumption and less area for SRAMs, 4T SRAM structure can be used. The 4T SRAM suffers low static noise margin (SNM) and other stability issues compared with commonly used 6T SRAM. Few techniques can be used to improve the SNM and stability of 4T SRAM. In this project these techniques are implemented on a 4T SRAM cache and results are verified.

**Objective:**

The objective of this project is to design a cache memory using 4T SRAM and compare it with conventional 6T SRAM cache for parameters like power, area, stability and speed of operation. Then implement different power reduction techniques on designed 4T SRAM cache to get a optimized high speed memory block for low power applications.